CLAIMS

1. A non-volatile memory device comprising:

a plurality of non-volatile memory cells including a first array for storing self-test instructions and a second array for storing data values; and

a control circuit including a command register for receiving the self-test instructions from the first memory during a first operating phase, and a comparator circuit for detecting defective non-volatile memory cells in the second array by comparing the data values with predefined values during a second operating phase.

2. The non-volatile memory device according to Claim 1, further comprising:

an address buffer for generating row address signals and column address signals;

a row decoder for receiving the row address signals, and for accessing a row of said plurality of non-volatile memory cells that is identified by the row address information; and

a test mode register for storing a row address code, the test mode register being connected to the address buffer such that the address buffer generates the row address signals in response to the row address code.

3. The non-volatile memory device according to Claim 2, further comprising:

a column decoder for receiving the column address signals generated by the address buffer, and for accessing a column of said plurality of non-volatile memory cells that is identified by the column address signals; and

a counter for storing a column address code, the counter being connected to the address buffer such that the address buffer generates the column address signals in response to the column address code.

4. The non-volatile memory device according to Claim 1, further comprising:

an address buffer for generating address signals;

a decoder for receiving the address signals generated by the address buffer, and for accessing a group of said plurality of non-volatile memory cells that is identified by the address signals; and

a counter for storing an address code, the counter being connected to the address buffer such that the address buffer generates the address signals in response to the address code,

wherein the counter increments the address code in response to control signals generated by the control circuit.

5. The non-volatile memory device according to Claim 1, further comprising:

an output controller for registering the self-test instructions read from the first array during the first operating phase; and

a data bus connected between the output controller and the control circuit for transmitting the self-test instructions to the command register during the first operating phase.

6. The non-volatile memory device according to Claim 5, further comprising a data input buffer connected to the data bus and controlled by the control circuit such that data values received by the data input buffer are selectively passed to the command register.

7. A method for performing wafer sort testing on a non-volatile memory device using a tester, the non-volatile memory array including a first array of non-volatile memory cells, a second array of non-volatile memory cells, and a control circuit, the method comprising:

storing a series of self-test instructions transmitted from the tester in the first array of the non-volatile memory device, the series of self-test instructions including a first instruction and a second instruction;

reading the first instruction from the first array and transferring the first instruction to a command register of the control circuit, wherein the first instruction includes a pre-determined data pattern; and

writing the predetermined data pattern to a second array of non-volatile memory cells in accordance with the first instruction stored in the command register.

8. The method according to Claim 7, further comprising storing a first address code transmitted from the tester,

wherein reading the first instruction includes transmitting the first address code to an addressing circuit, whereby the addressing circuit accesses and reads the first instruction from the first array.

9. The method according to Claim 8, wherein writing the predetermined data pattern to the second array comprises transmitting control signals from the control circuit to the addressing circuit that cause the addressing circuit to sequentially access each of the non-volatile memory cells of the second array.

10. The method according to Claim 9, wherein writing the predetermined data pattern further comprises transmitting the predetermined data pattern to the addressing circuit such that the predetermined data pattern is repeatedly written into the sequentially accessed non-volatile memory cells.

11. The method according to Claim 7, further comprising:

transferring the second instruction from the first array to the command register of the control circuit, the second instruction including a predetermined data pattern; and

reading data values from the second array of non-volatile memory cells in accordance with the second instruction; and

comparing the data values read from the second array with the predetermined data pattern stored in the command register.

12. The method according to Claim 7,

wherein storing the series of self-test instructions comprises writing the series of self-test instructions into sequentially addressed non-volatile memory cells of the first array,

wherein the method further comprises storing a first address code transmitted from the tester in a counter,

wherein reading the first instruction includes transmitting the first address code from the counter to an addressing circuit, whereby the addressing circuit accesses and reads the first self-test instruction from the first array, and

wherein reading the second instruction includes incrementing the counter to generate a second address code, and transmitting the second address code from the counter to the addressing circuit.

13. The method according to Claim 7, further comprising storing a start self-test command transmitted from the tester in the command register, wherein the first instruction is read from the first array in response to the stored start self-test command.

14. The method according to Claim 7, further comprising transmitting status data to the tester.

15. A method for performing wafer sort testing on a non-volatile memory device using a tester, the non-volatile memory array including a first array of non-volatile memory cells, a second array of non-volatile memory cells, and a control circuit, the method comprising:

storing a self-test instruction transmitted from the tester in the first array of the non-volatile memory device;

reading the self-test instruction from the first array and transferring the self-test instruction to a command register of the control circuit, wherein the self-test instruction includes a predetermined data pattern;

reading data values from the second array of non-volatile memory cells in accordance with the self-test instruction; and

comparing the data values read from the second array with the predetermined data pattern.

16. The method according to Claim 15, further comprising storing an address code transmitted from the tester,

wherein reading the self-test instruction includes transmitting the address code to an addressing circuit, whereby the addressing circuit accesses and reads the self-test instruction from the first array.

17. The method according to Claim 16, wherein reading the data values from the second array comprises transmitting control signals from the control circuit to the addressing circuit that cause the addressing circuit to sequentially access each non-volatile memory cell of the second array.

18. The method according to Claim 7, wherein comparing the data values read from the second array with the predetermined data pattern further comprises transmitting the data values and the predetermined data pattern to a comparator.

19. A method for performing wafer sort testing on a non-volatile memory array comprising:

writing a series of self-test instructions into first memory cells of the non-volatile memory array;

transmitting a start command that causes the non-volatile memory array to sequentially read the series of self-test instructions from the first memory cells, and to execute the self-test instructions; and

receiving result data indicating completion of the series of self-test instructions from the non-volatile memory array,

wherein executing the series of self-test instructions by the non-volatile memory array involves writing at least one pattern into second memory cells of the non-volatile memory array, reading data from the second memory cells, and comparing the read data with said at least one pattern to detect malfunctioning second memory cells.

20. The method according to Claim 19, further comprising reading and verifying the series of self-test instructions from the first memory cells before transmitting the start command.